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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Malone — Art Unit: 2873

Serial No.: 10/036,696 — Examiner: Thomas, Brandi N.

Filed: 31 December 2001 — Docket No. TI-29278

For: LAMINATED PACKAGE

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___	DIVISIONAL APP'N	___	

NAME OF INVENTOR(S): Malone	RECEIPT DATE & SERIAL NO.: Application No.: 10/036,696
TITLE OF INVENTION: Laminated Package	**Filing Date:** 12/31/2001
TI FILE NO.: TI-29278 / DEPOSIT ACCT. NO.: **20-0668**	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPEAL BRIEF TRANSMITTAL

22 November 2004

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Transmitted herewith is an Appeal Brief in the above-identified application.

Please charge the $340.00 fee for filing the Brief to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Charge any additional fees, or credit overpayment to Deposit Account No. 20-0668.

Respectfully submitted,

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

22 November 2004

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Charles A. Brill — 22 Nov. 2004

Charles A. Brill — Date

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed 20 May 2004. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

This application was filed on 31 December 2001 with thirty six claims, seven of which were written in independent form. Claims 8-15 and 22-36 have been withdrawn from consideration as being drawn to a non-elected invention.

Claim 4 was canceled and Claims 3, 16-18, 20, and 21 were amended on 20 February 2004. Claims 1, 2, and 16 were amended by an amendment after the final rejection filed on 20 August 2004. The applicant appeals the rejection of Claims 1-3, 5-7, and 16-21.

STATUS OF THE AMENDMENTS

An amendment after the final rejection was filed on 20 August 2004. No response to that amendment has been mailed by the Examiner. The claims listed in the appendix hereto are submitted under the assumption that the amendment has been entered as its entry was not refused.

SUMMARY OF CLAIMED SUBJECT MATTER

Line 19 of page 2 of the specification, through line 5 of page 3 states one of the problems the present invention addresses. Namely, the small size of a micromirror array makes the alignment of the array critical to the performance of the device. A misalignment of only 100 μm shifts the image more than eight image pixels. The micromirror package is used to align the micromirror array to the display system optics. Not only must the micromirror be precisely aligned relative to the package, the plane of the micromirror must be aligned with the plane of the projection lens to achieve proper focus across the entire micromirror array.

Lines 2-11 of page 9 of the specification further describe embodiments of the present invention. "A method and system for precision micromirror alignment has been developed. The new method and system provide improved alignment of the micromirror device to display system optics. The improved alignment is achieved by exposing portions of a reference layer of the package substrate. When the micromirror is packaged, it is placed on the reference layer. The reference layer is used to position the micromirror relative to the display optics, especially the projection lens. The surface of the same reference layer both supports the micromirror and positions the package relative to the optics. This removes the tolerance build up accumulated by the intervention of package layers formed on top of, or beneath, the reference layer. The removal of this tolerance build-up provides improved control over the back focal length of the projection lens and improves the image focus over the entire surface of the micromirror array."

Figure 10, in combination with line 17 of page 14 through line 7 of page 15, and lines 15-20 of page 4, teach embodiments of the invention recited by Claim 1.

Figures 4 and 5, in combination with line 4 of page 11 through line 22 of page 12, and lines 11-14 of page 5 teach embodiments of the invention recited by Claim 16.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether Claims 1-3, 5-7, and 16-21 are unpatentable under 35 U.S.C. § 103 (a) over U.S. Patent No. 4,954,480 to Imanaka *et al.* in view of U.S. Patent No. 6,326,244 to Brooks *et al.*

ARGUMENT

Ground of Rejection 1:

Whether Claims 1-3, 5-7, and 16-21 are unpatentable under 35 U.S.C. § 103 (a) over U.S. Patent No. 4,954,480 to Imanaka *et al.* ("Imanaka") in view of U.S. Patent No. 6,326,244 to Brooks *et al.* ("Brooks").

"A person shall be entitled to a patent unless," creates an initial presumption of patentability in favor of the applicant. 35 U.S.C. § 102. "We think the precise language of 35 U.S.C. § 102 that, 'a person shall be entitled to a patent unless,' concerning novelty and unobviousness, clearly places a burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103, see Graham and Adams." *In re Warner*, 379 F.2d 1011, 1016 (C.C.P.A. 1967) (referencing *Graham v. John Deere Co.*, 383 U.S. 1 (1966) and *United States v. Adams*, 383 U.S. 39 (1966)). "As adapted to *ex parte* procedure, *Graham* is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'." *In re Piasecki*, 745 F.2d 1468 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d at 1016).

"The prima facie case is a procedural tool which, as used in patent examination (as by courts in general), means not only that the evidence of the prior art would reasonably allow the conclusion the examiner seeks, but also that the prior art compels such a conclusion if the applicant produces no evidence or argument to rebut it." *In re Spada*, 911 F.2d 705, 708 n.3 (Fed. Cir. 1990).

"Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the

level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy." Graham v. Deere, 383 U.S. 1, 17-18 (1966).

"To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985).

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). 'All words in a claim must be considered in judging the patentability of that claim against the prior art.' In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.

Claim 1:

Claim 1 was rejected under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent No. No. 6,310,650 to Johnson et al. ("Johnson") in view of U.S. Patent No. 5,485,279 to Yonemitsu et al. ("Yonemitsu"). The applicant respectfully disagrees and submits the Examiner has failed to present a prima facie case of obviousness as required.

Claim 1 recites, "A method of forming a package substrate, the method comprising: providing sheets of substrate layers; forming metalized patterns on at least one of said sheets; laminating said sheets to form said package substrate, said sheets shaped to provide a substrate having a cavity, said cavity defining a reference plane, wherein said layers are shaped to expose limited regions of said reference plane outside said cavity; and separating said laminated sheets to form individual package substrates."

The Examiner has the duty to present a prima facie obviousness rejection. Under Graham, this requires determining the differences between the prior art and the claims at issue. The Examiner stated, Imanaka et al. teaches a method of forming a package substrate . . . except that it does not show . . . a cavity having a floor defining a reference plane." "Brooks et al. shows that it is known to provide a cavity formed in the substrate having a floor defining a reference plane, wherein said layers are shaped to expose limited regions of said reference plane outside said cavity for permitting the use of a flexible, tape-type base laminate in the package (col. 4, lines 23-30)."

Brooks, in lines 23-38 of column 4, states, "In one embodiment, the reference place [sic] element is also formed as a frame of like size and shape to the adhesive frame, and placed thereover in alignment therewith, providing a deepened cavity. It should be noted that the use of a relatively thick, and thus rigid, reference plane element permits the use of a flexible, tape-type base laminate in the package, and also provides additional mass to facilitate heat transfer from the semiconductor die. After the semiconductor die is back-bonded to the die-attach location on the base laminate, connections are formed between the traces and the bond pads of the die, after which the die, inner trace ends and connections may be encapsulated with a so-called 'glob top' of dielectric material,

providing physical and environment protection for the encapsulated elements. The reference plane element and underlying adhesive provide a four-sided dam to prevent unwanted lateral encapsulant spread."

Thus, contrary to the Examiner's assertion, Brooks does not appear to show, teach, or suggest "sheets shaped to provide a substrate having a cavity, said cavity defining a reference plane, wherein said layers are shaped to expose limited regions of said reference plane outside said cavity" as recited by Claim 1.

Brooks merely teaches a "ground or other voltage reference plane element (hereinafter sometimes referenced generally as a "reference plane element") is secured to the adhesive layer. Various embodiments of the structure of the BGA package of the invention include differing reference plane element structures, which in turn also permit different die enclosure techniques. In each embodiment, however, the insulative layer over the traces is provided with at least one through hole for connection of one or more circuit traces to the reference plane element by mutual contact with the anisotropically conductive adhesive layer" (column 4, lines 12-22).

Brooks' "reference plane element" is identified as reference number 50 in Figures 1, 2, and 5 (column 6, lines 46-47), reference number 150 in Figure 3 (column 7, line 48), and reference number 250 in Figure 4 (column 8, line 3). A cursory review of these figures indicates the reference plane element of Brooks is a package lid and the package lid of Brooks, in combination with the teachings of Imanaka cannot be held to suggest to one of ordinary skill in the art, "providing sheets of substrate layers; forming metalized patterns on at least one of said sheets; laminating said sheets to form said package substrate, said sheets shaped to provide a substrate having a cavity, said cavity defining a

reference plane, wherein said layers are shaped to expose limited regions of said reference plane outside said cavity; and separating said laminated sheets to form individual package substrates" as recited by Claim 1.

The reference plane of Brooks simply is not defined by a cavity of a substrate provided by sheets shaped to provide the substrate having the cavity. Additionally, Imanaka in view of Brooks cannot be held to show, teach, or suggest "sheets of substrate layers" "wherein said layers are shaped to expose limited regions of said reference plane outside said cavity."

Furthermore, there is no suggestion in the prior art of record that suggests the modification or combination of references suggested by the Examiner. Additionally, the Examiner has failed to present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references as required by *Ex parte Clapp*.

To the contrary, the Examiner merely states, "It would have been obvious to one of ordinary skill in the art at the time the inventions was made to separate the sheets to form individual package substrates for the purpose of aligning and precisely positioning the micromirrors." How the forming individual packages advances the "purpose of aligning and precisely positioning the micromirrors" is not taught by the Examiner, nor is it at all clear to the applicant. It appears the Examiner simply took a claim feature admitted as not taught by the prior art reference and combined it with an unrelated advantage mentioned in the specification to provide a thinly veiled appearance of a suggestion to modify the art.

The Examiner further compounds the fallacy by stating, "Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Imanaka et al. with the cavity and reference plane of Brooks et al. for the purpose of permitting the use of a flexible, tape-type base laminate in the package (col. 4, lines 23-30)." Here the Examiner has taken the "teachings" of one reference and combined them with a claim feature not taught by either reference justified the combination as achieving the purposes taught by a second reference. While the package lid Brooks calls a "reference plane element" clearly does not meet the limitations of a reference plane as described in the claims or the specification, the combination with Imanaka allegedly is justified by the benefits the package lid provides to Brooks' package—regardless of the applicability of either the package lid or Brooks' desired benefits to Imanaka's package. The cited passage from Brooks basically teaches that a rigid package lid obviates the need for a rigid package substrate—a teaching that is irrelevant to the present invention and fails to provide any suggestion to combine or modify either Imanaka or Brooks.

The Examiner therefore has not met the burden of presenting a prima facie case of obviousness, and the rejection under 35 U.S.C. § 103(a) is defective and should be withdrawn.

Claim 16:

Claim 16 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Imanaka in view of Brooks. The applicant respectfully disagrees and submits, the

Examiner has failed to present a prima facie case of obviousness, and the rejection under 35 U.S.C. § 103(a) is defective and should be withdrawn.

Claim 16 recites, "A package substrate, comprising: a first surface; a second surface opposing said first surface; a cavity open to said second surface, said cavity defining a reference plane; and regions outside said cavity exposing a discrete portions of a surface of said reference plane."

The Examiner has the duty to present a prima facie obviousness rejection. Under Graham, this requires determining the differences between the prior art and the claims at issue. The Examiner stated, Imanaka et al. discloses a package substrate, comprising: a first surface (3 and 5, insulating layers); a second surface opposing said first surface (2) but does not disclose a cavity open to said second surface, said cavity having a floor defining a reference plane; and regions outside said cavity exposing a discrete portions of a surface of said reference plane. Brooks et al. shows that it is known to provide a cavity open to said second surface, said cavity having a floor defining a reference plane; and regions outside said cavity exposing a discrete portions of a surface of said reference plane for permitting the use of a flexible, tape-type base laminate in the package (col. 4, lines 23-30)."

Brooks, in lines 23-38 of column 4, states, "In one embodiment, the reference place [sic] element is also formed as a frame of like size and shape to the adhesive frame, and placed thereover in alignment therewith, providing a deepened cavity. It should be noted that the use of a relatively thick, and thus rigid, reference plane element permits the use of a flexible, tape-type base laminate in the package, and also provides additional mass to facilitate heat transfer from the semiconductor die. After the semiconductor die is

back-bonded to the die-attach location on the base laminate, connections are formed between the traces and the bond pads of the die, after which the die, inner trace ends and connections may be encapsulated with a so-called 'glob top' of dielectric material, providing physical and environment protection for the encapsulated elements. The reference plane element and underlying adhesive provide a four-sided dam to prevent unwanted lateral encapsulant spread."

Thus, contrary to the Examiner's assertion, Brooks does not appear to show, teach, or suggest "a cavity open to said second surface, said cavity having a floor defining a reference plane; and regions outside said cavity exposing a discrete portions of a surface of said reference plane" as recited by Claim 16.

Brooks merely teaches a "ground or other voltage reference plane element (hereinafter sometimes referenced generally as a "reference plane element") is secured to the adhesive layer. Various embodiments of the structure of the BGA package of the invention include differing reference plane element structures, which in turn also permit different die enclosure techniques. In each embodiment, however, the insulative layer over the traces is provided with at least one through hole for connection of one or more circuit traces to the reference plane element by mutual contact with the anisotropically conductive adhesive layer" (column 4, lines 12-22).

Brooks' "reference plane element" is identified as reference number 50 in Figures 1, 2, and 5 (column 6, lines 46-47), reference number 150 in Figure 3 (column 7, line 48), and reference number 250 in Figure 4 (column 8, line 3). A cursory review of these figures indicates the reference plane element of Brooks is a package lid and the package lid of Brooks, in combination with the teachings of Imanaka cannot be held to suggest to

one of ordinary skill in the art, "A package substrate, comprising: a first surface; a second surface opposing said first surface; a cavity open to said second surface, said cavity defining a reference plane; and regions outside said cavity exposing a discrete portions of a surface of said reference plane" as recited by Claim 16.

Furthermore, there is no suggestion in the prior art of record that suggests the modification or combination of references suggested by the Examiner. Additionally, the Examiner has failed to present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references as required by *Ex parte Clapp*.

To the contrary, the Examiner merely states, "it would have been obvious to someone of ordinary skill in the art at the time the inventions was made to combine the teaching of Imanaka et al. with the cavity and reference plane of Brooks et al. for the purpose of permitting the use of a flexible, tape-type base laminate in the package (col. 4, lines 23-30)." Here the Examiner has taken the "teachings" of one reference and combined them with a claim feature not taught by either reference justified the combination as achieving the purposes taught by a second reference. While the package lid Brooks calls a "reference plane element" clearly does not meet the limitations of a reference plane as described in the claims or the specification, the combination with Imanaka allegedly is justified by the benefits the package lid provides to Brooks' package—regardless of the applicability of either the package lid or Brooks' desired benefits to Imanaka's package. The cited passage from Brooks basically teaches that a rigid package lid obviates the need for a rigid package substrate—a teaching that is

irrelevant to the present invention and fails to provide any suggestion to combine or modify either Imanaka or Brooks.

The Examiner therefore has not met the burden of presenting a prima facie case of obviousness, and the rejection under 35 U.S.C. § 103(a) is defective and should be withdrawn.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-3, 5-7, and 16-21 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) A method of forming a package substrate, the method comprising:

providing sheets of substrate layers;

forming metalized patterns on at least one of said sheets;

laminating said sheets to form said package substrate, said sheets shaped to provide a substrate having a cavity, said cavity defining a reference plane, wherein said layers are shaped to expose limited regions of said reference plane outside said cavity; and

separating said laminated sheets to form individual package substrates.

2. (Previously presented) The method of Claim 1, wherein said laminating said sheets comprises laminating said sheets to form said package substrate, said sheets shaped to provide a substrate having a cavity surrounded by a substrate wall, said cavity defining a reference plane, wherein said sheets are shaped to expose regions of said reference plane outside said substrate wall.

3. (Previously presented) The method of Claim 1, wherein said laminating said sheets comprises laminating said sheets to form said package substrate, said sheets shaped to expose regions of said reference plane to a surface of said package substrate parallel to said reference plane.

4. (Canceled)

5. (Original) The method of Claim 1, said forming metalized patterns on at least one of said sheets comprising forming metalized patterns on at least one of said sheets to provide electrical connection between said cavity and an external surface of said package substrate.

6. (Original) The method of Claim 1, said providing substrate sheets comprising:

providing ceramic substrate sheets.

7. (Original) The method of Claim 1, said providing substrate sheets comprising:

providing plastic substrate sheets.

8. (Withdrawn) A method of packaging a semiconductor device, the method comprising:

providing a package substrate, said package substrate having a cavity,

said cavity having a floor defining a reference plane, surface regions of said reference plane exposed outside said cavity;

attaching a semiconductor device in said cavity of said package substrate;

attaching a lid to said package substrate to enclose said device in said cavity.

9. (Withdrawn) The method of Claim 8, said providing a package substrate comprising:

providing a package substrate, said regions of said reference plane exposed outside said cavity to a top surface of said package.

10. (Withdrawn) The method of Claim 8, said providing a package substrate comprising:

providing a package substrate, said regions of said reference plane exposed to a bottom surface of said package.

11. (Withdrawn) The method of Claim 8, said attaching a semiconductor device comprising:

attaching an electro-optical device in said cavity.

12. (Withdrawn) The method of Claim 8, said attaching a semiconductor device comprising:

attaching a micromirror device in said cavity.

13. (Withdrawn) A method of aligning a display system, the method comprising:

providing positioning structures defining a display system reference plane;

aligning a micromirror package with said display system reference plane, said micromirror package having a reference plane defined by regions on a common plane, a micromirror attached to at least one of said regions, said alignment of said micromirror package accomplished by placing at least two of said regions defining said reference plane against said positioning structures;

positioning illumination optics relative to said display system reference plane; and

positioning projection optics relative to said display system reference plane.

14. (Withdrawn) The method of Claim 13, wherein said illumination optics comprises a prism, said aligning a micromirror package and said positioning illumination optics comprising:

positioning said micromirror package against a mount, said mount contacting said regions on said micromirror package reference plane; and

positioning said prism against said mount.

15. (Withdrawn) A method of aligning an optical system, the method comprising:

providing positioning structures defining an optical system reference plane;

aligning a optical device package with said optical system reference plane, said optical device package having a reference plane defined by regions on a common plane, an optical device attached to at least one of said regions, said alignment of said optical device package accomplished by placing at least two of said regions defining said reference plane against said positioning structures; and

positioning optics relative to said optical system reference plane.

16. (Previously presented) A package substrate, comprising:

a first surface;

a second surface opposing said first surface;

a cavity open to said second surface, said cavity defining a reference plane; and

regions outside said cavity exposing a discrete portions of a surface of said reference plane.

17. (Previously presented) The package substrate of Claim 16, wherein said regions outside said cavity expose a surface of said reference plane from a side corresponding to said second surface.

18. (Previously presented) The package substrate of Claim 16, wherein said regions outside said cavity expose a surface of said reference plane from a side corresponding to said first surface.

19. (Original) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said regions formed by voids in said layers on one side of said reference plane.

20. (Previously presented) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a side of said reference plane corresponding to said second surface.

21. (Previously presented) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a side of said reference plane corresponding to said first surface.

22. (Withdrawn) A packaged semiconductor device, comprising:

a package substrate, said package substrate having a cavity, said cavity having a floor defining a reference plane, discrete regions of said reference plane exposed outside said cavity;

a semiconductor device in said cavity of said package substrate;

a lid attached to said package substrate enclosing said device in said cavity.

23. (Withdrawn) The packaged semiconductor device of Claim 22, wherein said

19. (Original) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said regions formed by voids in said layers on one side of said reference plane.

20. (Previously presented) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a side of said reference plane corresponding to said second surface.

21. (Previously presented) The package substrate of Claim 16, said package substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a side of said reference plane corresponding to said first surface.

22. (Withdrawn) A packaged semiconductor device, comprising:

a package substrate, said package substrate having a cavity, said cavity having a floor defining a reference plane, discrete regions of said reference plane exposed outside said cavity;

a semiconductor device in said cavity of said package substrate;

a lid attached to said package substrate enclosing said device in said cavity.

23. (Withdrawn) The packaged semiconductor device of Claim 22, wherein said regions outside said cavity expose a surface of said reference plane from a top side.

24. (Withdrawn) The packaged semiconductor device of Claim 22, wherein said regions outside said cavity expose a surface of said reference plane from a bottom side.

25. (Withdrawn) The packaged semiconductor device of Claim 22, said package substrate formed of a laminated series of layers, said regions formed by voids in said layers on one side of said reference plane.

26. (Withdrawn) The packaged semiconductor device of Claim 22, said package substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a top side of said reference plane.

27. (Withdrawn) The packaged semiconductor device of Claim 22, said package

substrate formed of a laminated series of layers, said cavity and said regions formed by voids in said layers on a bottom side of said reference plane.

28. (Withdrawn) The packaged semiconductor device of Claim 22, said semiconductor device being an electro-optical device.

29. (Withdrawn) The packaged semiconductor device of Claim 22, said semiconductor device being a micromirror device.

30. (Withdrawn) A display system, comprising:

positioning structures defining a display system reference plane;

a spatial light modulator package having a reference plane defined by discrete regions on a common plane, a spatial light modulator attached to at least one of said regions, at least two of said regions of said spatial light modulator package against said positioning structures;

illumination optics positioned relative to said display system reference plane; and

projection optics positioned relative to said display system reference plane.

31. (Withdrawn) The display system of Claim 30, said illumination optics comprising a prism, further comprising:

a mount contacting said regions on said spatial light modulator package reference plane and said prism.

32. (Withdrawn) The display system of Claim 30, said positioning structures connected to a system chassis, wherein said illumination optics and said projection optics are positioned relative to said display chassis.

33. (Withdrawn) The display system of Claim 30, said positioning structures comprising structured formed in said system chassis, wherein said illumination optics and said projection optics are positioned relative to said display chassis.

34. (Withdrawn) The display system of Claim 30, said positioning structures comprising structured formed in said system chassis, wherein said illumination optics and said projection optics are positioned relative to preformed features in said display chassis.

35. (Withdrawn) The display system of Claim 30, said spatial light modulator being a

micromirror device.

36. (Withdrawn) The display system of Claim 30, said spatial light modulator being a liquid crystal on silicon device.